REMARKS/ARGUMENTS

Claims 1-24 were pending in the present application. By virtue of this response, claims 1 and 10 have been amended. Accordingly, claims 1-24 are currently under consideration. Amendment of certain claims is not to be construed as a dedication to the public of any of the subject matter of the claims as previously presented. No new matter has been added.

Rejections under 35 U.S.C § 112, First Paragraph

Claims 5 and 14 are rejected under 35 U.S.C § 112, first paragraph. The Examiner asserted that "the term 'in-flight' is not established in the art, does not enable one of ordinary skill in the art to practice or understand the invention. An artisan would be unable to assign the 'in-flight' field without further detail as to its definition." (OA, paragraph 4.)

This rejection is respectfully traversed. The Examiner's attention is respectfully directed to the Specification. The Specification clearly states that a "packet is considered to be in-flight when the packet is being processed, such as if a packet is being read out of memory, being sent out onto the bus, and the like." (Specification, page 14, lines 6-7.) Reconsideration of claims 5 and 14 is requested.

Rejections under 35 U.S.C § 112, Second Paragraph

Claims 1, 7 and 10 are rejected under 35 U.S.C § 112, second paragraph. The term "Data Memory Access (DMA)" in claims 1 and 10 has been amended to read "Direct Memory Access (DMA)." The text of the title and detailed description has similarly been amended. It is believed that claim 7, which reference only "DMA" and ultimately depends on independent claim 1, does not require amendment. Reconsideration of claims 1, 7 and 10 is requested.

Rejections under 35 U.S.C § 101

Claim 9 is rejected under 35 U.S.C § 101. The Examiner states that "the shift structure as

taught by the invention could not be embodied as a FIFO device. A FIFO device by definition is processed in a very linear fashion. The first object added is the first object removed, not allowing for shifting, or sorting." (OA, paragraph 10.)

The rejection is respectfully traversed. Claim 9 recites "wherein said shifting structure is a First-In-First-Out (FIFO) device." The first definition of FIFO in the New IEEE Standard Dictionary of Electrical and Electronics Terms, Fifth Edition, is:

> A technique for managing a set of items to which additions and deletions are to be made; items are appended to one end of a list and retrieved from the other end.

Note that this definition of FIFO does not preclude the shifting of entries in a FIFO as asserted by the Examiner. Consistent with this definition of FIFO, the FIFO described in the present specification has an end, where data enters, and a head, where data leaves. (See entries 606 and 619, respectively, in Fig. 6.) A new entry enters the FIFO at the end of the FIFO. See Fig. 9, which shows that an "entry 617 can be written to the end of shift structure 600." (Specification, page 17, line 23 to page 18, line 1.) When a system is ready to take an entry from the FIFO, the entry at the head of the FIFO will be taken. Each entry in the FIFO will eventually be read and leave the FIFO from the head of the FIFO. (See Specification, page 16, line 11 to page 17, line 2.) Therefore, reconsideration of claim 9 is requested.

Rejections under 35 U.S.C § 103

Claims 1-4, 10-13 and 19-24 are rejected under 35 U.S.C § 103 as being unpatentable over U.S. Patent 5,504,919 ("Lee") in view of U.S. Patent 6,052,375 ("Bass").

With regard to claim 1, the Examiner cites to Lee's Figure 2 and abstract and states "Lee teaches a shift structure having a plurality of entries, and a comparison logic circuit to sort the entries based on their respective weights." The Examiner further states that "Bass teaches a scheduler for DMA channels data transfer. Bass teaches a plurality of fields in a parameter table ... Bass further teaches that queues are sorted for output to a traffic queue allocation manager." (OA,

paragraph 12.)

The rejection is respectfully traversed. First, neither cited reference discloses "wherein each entry includes a weight that is determined based on said plurality of fields" as recited in claim 1. Lee does not determine a weight based on a plurality of fields. In fact, an entry of Lee includes just a single value. (See Lee's Figure 1B.) The Examiner cites to Bass (column 4, line 46 to column 5, line 38), which describes a list of parameters in a TSPT table. The Examiner notes that Bass does not use the term weights, but asserts that "the term weight and priority are interchangeable in this context." Applicants assert that the priorities (i.e., high-regulated priority (H), low-regulated priority (L), and unregulated priority (U)) do not function as the weights recited in claim 1. More particularly, claim 1 recites that the weight "is determined based on said plurality of fields." Bass does not disclose that the priorities are determined based on the parameters in the TSPT table.

Second, neither cited reference discloses a circuit "to sort said entries based on their respective weights" as recited in claim 1. The Examiner cites to Bass, which states "[i]n each output port, the selected input queues are sorted and multiplexed by the traffic queue allocation manager." (Bass, Column 5, lines 42-44.) Bass does not describe sorting a plurality of entries within a queue but rather describes its sorting of input from input queues (labeled 10 in Bass' Figure 2 and labeled Q0-Q31 in Bass' Figures 1, 2 and 9). Bass routes entries from 32 input queues to 18 output ports (each of the 18 output ports having 3 priority queues for a total of 54 port queues) to 3 global priority queues. Specifically, Bass states "each of the 32 input logic queues 10 [are fed] to 18 output ports." (Bass, column 5, lines 39-42.) Bass continues stating:

> Each port has three selected out-port queues (Hx, Lx, Ux). The Hx out-port queues of each port are fed to a H-port-priority-arbiter 20. The Lx out-port queues of each port are fed to an L-port-priority-arbiter 21. The Ux out-port queues of each port are fed to a U-port-priority-arbiter 22. The three port arbiters arbitrate all the corresponding out-port queues into three selected out-port queues. These three selected out-port priority queues are then fed to a DMA bus arbiter 23 which arbitrates the selected out-port priority queues in a straight priority fashion.
> (Bass, column 5, lines 53-63.)

In other words, sorting in Bass occurs by routing input from each of 32 input queues to a selected one of 54 different queues. The selection may be based on priority (H, L, U) and port (Port

0-Port17). Finally, input from the 54 different queues (18 Hx + 18 Lx + 18 Ux) are routed to three global priority queues.

Third, there is no motivation to combine Lee and Bass. Bass disclose a number of queue to which input is routed. More particularly, in Bass the queues are already filtered with data of the same level of priority. For example, the 18 Hx port queues only have H-priority data. Thus, sorting the entries, using the sorting structure disclosed in Lee or any other sorting structure, in a queue having with the same priority based on their priority would not serve a purpose.

Therefore, reconsideration and allowance of claim 1 are requested.

The Examiner rejects claims 10 and 19 with similar arguments. Claims 10 and 19 are each methods of scheduling multiple channels. The rejections are similarly traversed. The combination of Lee and Bass discloses neither the method of claim 10 nor the method of claim 19. Claim 10 recites "writing ... entries in a shift structure," "assigning weights" and "sorting said entries based on said weights, wherein an entry having the highest weight is sorted to the head of said shift structure." As described with reference to claim 1, Bass sorts input queues into a number of priority queues. Once the input queue is routed to a priority queue, there is nothing left in Bass' queue to sort. In sum, neither Bass nor Lee discloses assigning weights or sorting entries based on weights. Reconsideration and allowance of claims 10 and 19 are requested.

Regarding the remaining rejected claims (dependent claims 2-4, 11-13 and 20-24), each ultimately depends on an independent claim shown to be allowable. Reconsideration and allowance of dependent claims 2-4, 11-13 and 20-24 as well as independent claims 1, 10 and 19 are requested.

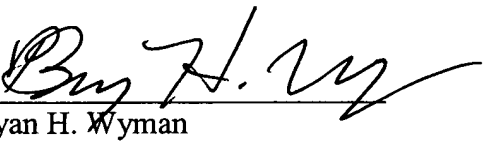
CONCLUSION

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejections of the claims and to pass this application to issue. If it is determined that a telephone conversation would expedite the prosecution of this application, the Examiner is invited to telephone Peter Yim at (415) 268-6373 or the undersigned at the number given below.

In the unlikely event that the transmittal letter is separated from this document and/or the Patent Office determines that an extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Assistant Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952** referencing docket no. 388682000400. However, the Assistant Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

Dated: August 11, 2003

Respectfully submitted,

By 

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